ABSOLUTE BINARY PROGRAM NO. 12621-16001
DATE CODE 1532

HP 12621A RECEIVE SYNCHRONOUS DATA SET INTERFACE DIAGNOSTIC

(PART OF 12618A TRANSMIT-RECEIVE SYNCHRONOUS INTERFACE KIT)

reference manual

For HP 2100 Series Computers

HEWLETT-PACKARD COMPANY
11000 WOLFE ROAD, CUPERTINO, CALIFORNIA, 95014

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HP 2100 SERIES RECEIVE (ONLY) INTERFACE (12621A) DIAGNOSTIC

INTRODUCTION

This diagnostic program confirms proper operation of the HP 12621A Receive (only) Interface Kit with an HP 2100 Series Computer. The program is designed for maximum testing speed. The operator may repeat each function test within the diagnostic as often as desired; or he may run the entire program, stopping after each test to evaluate the results.

REQUIRED HARDWARE

This diagnostic runs on an HP 2100A Series Computer and requires a test connector installed on the interface board during execution. Figure 1 shows how the test connector routes the board outputs to the inputs. Figure 2 shows the I/O word formats.

A console teleprinter is optional for reporting errors and messages to the operator. If a teleprinter is not available, errors and messages are reported by displays of MEMORY DATA error codes.

REQUIRED SOFTWARE

The following software is required:

Diagnostic Configurator product no. 24296A used for equipment configuration and as a console device driver.

Binary object tape	Part No. 24296-60001
Manual	Part No. 02100-90157

HP 12621A Receive Synchronous Data Set Interface Diagnostic binary object tape, Part No. 12621-16001.

REQUIRED SOFTWARE (cont.)

NOTE: The Diagnostic Serial Number (DSN) for the HP 12621A diagnostic, which resides in memory location 126_8 is 103012_8.

FUNCTIONAL AND OPERATIONAL CHARACTERISTICS

The Diagnostic Configurator must be loaded and configured prior to loading this diagnostic. Then this diagnostic program may be loaded and configured using the Switch Register. After the computer halts, all other program options (suppress printout, suppress halts, etc.) may be selected via the Switch Register as shown in Table 1. A copy of the configured program may be obtained by using the Diagnostic Configurator Dump routine, thereby avoiding a configuration process each time the diagnostic is used.

The diagnostic is started using instructions outlined under Operating Instructions. If an error is detected, the program prints a message on the teleprinter, then halts with a MEMORY DATA error code displayed. (Exceptions are trap cell halts $1060xx_8$ located in low memory 2_8 through 77_8, which do not print a message. The cause of any trap cell halt should be determined by the user before the diagnostic is restarted.) If a teleprinter is not available and the diagnostic halts, the MEMORY DATA display is checked against Table 2 information to determine the error or message. If a teleprinter is not available, data is displayed as a halt in the display register. All Halt messages are summarized in Table 2.

PROGRAM ORGANIZATION

The diagnostic consists of the routines described below:

CFGR — The Configuration routine configures the diagnostic for the proper select code (I/O channel).

PROGRAM ORGANIZATION (cont.)

INIT — The Initialization routine sets trap cell halts in locations 2_8 through 77_8 and prints the start-of-diagnostic message on the teleprinter.

BI/O — The Basic I/O routine begins by clearing the interface, checking all flag instructions and testing the ability to enable and disable interrupts. BI/O then tests the interrupt ability by forcing an interrupt, checking the return address for the correct location, and checking the interrupt acknowledge. BI/O checks the control reset functions, and, if that program option is selected, tests INTERNAL and EXTERNAL PRESET. When the PRESET switch(es) is (are) tested, BI/O checks for flag set, interrupts disabled, and control bit cleared.

NOTE: At the end of the BI/O section, and all of the following described routines (except END), the diagnostic tests program option bit 13 for a "repeat function" request.

FCTST — The Function/Status routine issues a function request to the interface then checks the Data/Status Word. (See Figure 2.) All combinations of functions requests, status returns, and flag setting conditions made possible through the test connector are tested.

RECVP — The Receive Pattern routine tests all data patterns possible for all character sizes in the no-parity, odd-parity, and even-parity modes. Data is issued one-bit-at-a-time on the SBA (reverse channel) line and the test clock is forced from a 1 to a 0 state. (See Figure 2.) For each data word transferred, the routine checks for the flag set and checks the Buffer Status and Error bits in the Data/Status Word.

SPCHR — The Special Character routine tests the ability of the interface to recognize as a special character all patterns possible for all word sizes in the no parity, odd parity and even parity modes. (See Figure 2.) A test is made with a special character selected and a non-special character received to show that the special character status bit will set only when a special character is sent to the interface. The flag set condition and the buffer ready and the special character status bits are tested for each data word transferred from the interface.

SYNCH — The Sync Character routine tests the ability of the interface to recognize and not ignore sync characters in the data when the SYNC FLAG option (bit 4 of the control word format) is ON. All patterns are tested for all word sizes and parities. (See Figure 2.)

LOCKN — The Lock-On Data routine simulates a data transfer by setting the sync pattern in the interface, sending non-sync data, and sending two sync patterns. The status is checked for the sync bit set and clear and for the flag remaining clear.

ERRFF — The Error Flip-Flop routine forces a parity error in both the even- and odd-parity modes, and tests the error bit (bit 8) in the Data/Status Word to see that the Error Flip-Flop is set. (See Figure 2.) Then ERRFF tests the error bit again by issuing two data patterns in the no-parity mode without clearing the flag between each transfer.

END — This routine prints the end-of-diagnostic message on the teleprinter, then tests program option bit 12 for a request to halt at the end of the complete diagnostic cycle.

LIMITATIONS

This diagnostic does not check the DMA (DCPC) portion of the interface nor the Request to Send Signal (CA, pin X) which must be tested with a voltage measuring device.

Of the four possible priority string errors that can exist in an interface board, only three can be tested for the HP 12621A Interface as follows:

1. Does the interface receive priority? Tested by this diagnostic.
2. Can the interface be denied priority? To make this test, the user must extract an unused higher-priority board, then run this diagnostic and expect a MEMORY DATA error code 102005_8, message E5. (See Table 2.)
3. Does the interface deliver priority? This is tested only by running a diagnostic for a lower priority interface board to some other device.
4. Can the interface deny priority? Not tested by this diagnostic.

OPERATING INSTRUCTIONS

a. Install the test connector (HP part number 12621-60005) on the interface.

b. Load and configure the Diagnostic Configurator.

c. Set starting address 000100_8.

d. Load this diagnostic program. Set the Switch Register to the select code of the device interface. Press RUN and wait for halt (MEMORY DATA is 102074_8). Set the Switch Register to the desired settings shown in Table 1, then press RUN. The program will start execution.

e. After the program has advanced through all the tests, a message indicates completion of the diagnostic program. The diagnostic will come to an orderly halt at the end of each test if bit 15 of the Switch Register is set or, end of diagnostic (102077_8) will occur. (To restart the diagnostic without reconfiguration, load address 2000_8). The operator may press RUN to make another pass.

MESSAGE ANALYSIS

All diagnostic messages printed on the teleprinter are prefixed by an alpha-numberic code. An H prefix indicates an operating instruction, while an E prefix signals an error message.

All halts display a MEMORY DATA error code. Refer to Table 2 to analyze the halt conditions, then press RUN to resume the diagnostic program.

If a trap cell halt occurs on the teleprinter channel, change program option bit 11 to suppress all teleprinter messages (See Table 1), then restart the diagnostic at location 2000_8.

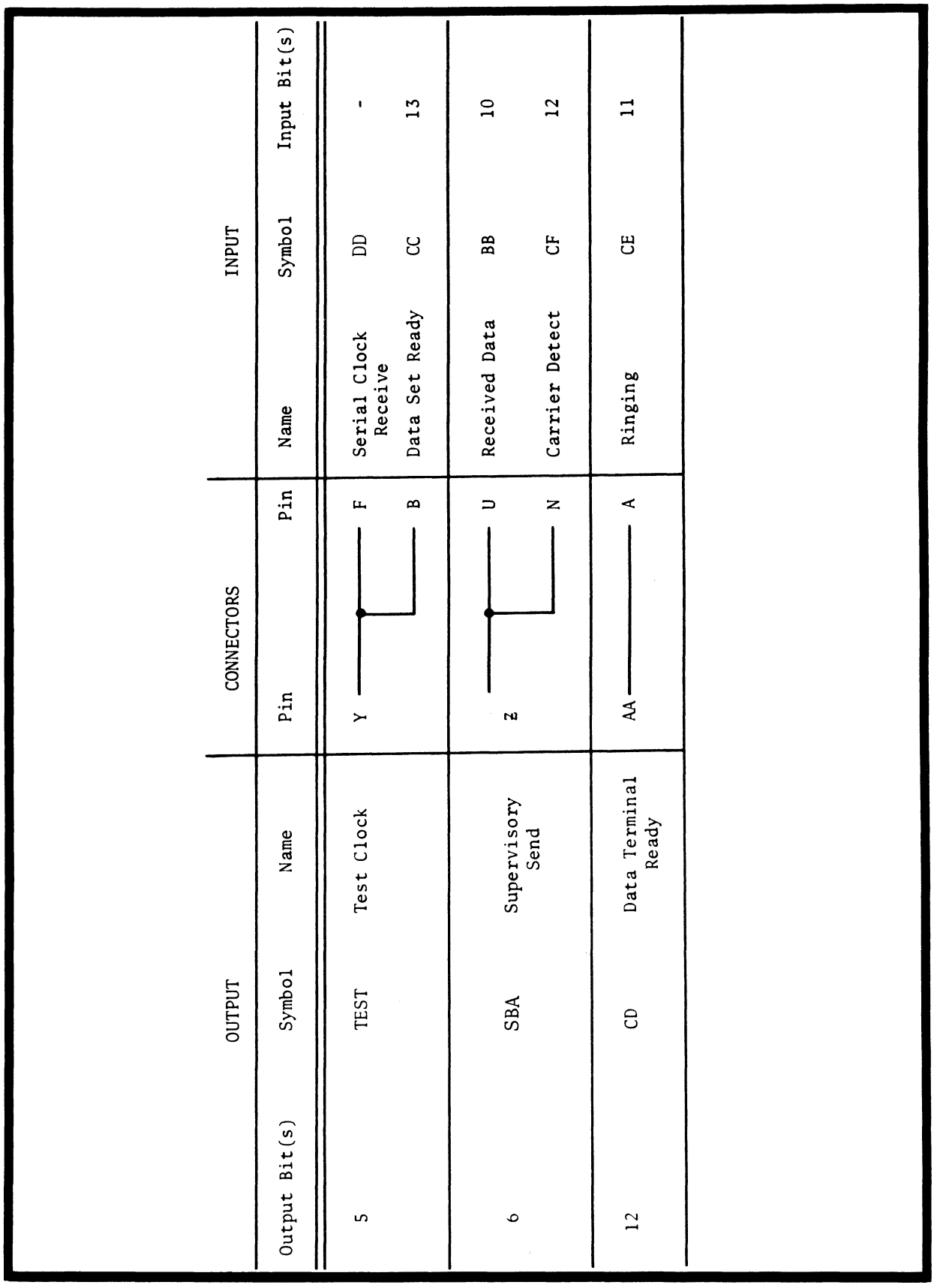

Figure 1. Test Connector (HP 12621-60005 Diagram

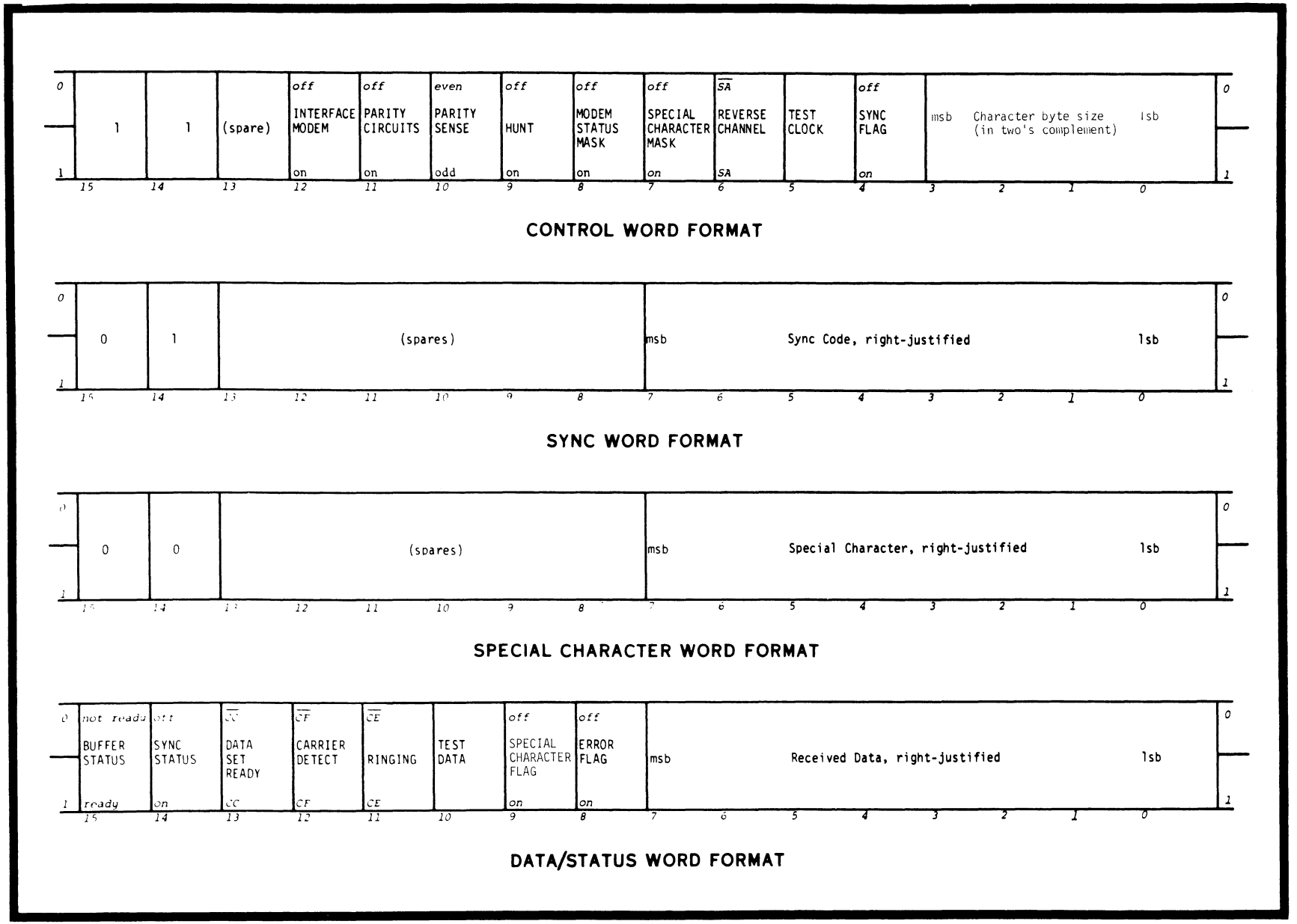

Figure 2. I/O Word Formats

Table 1. Program Options--Switch Register Settings

SWITCH REGISTER

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits	Functions
0-8	Spares
9	Set on to suppress start and stop messages.
10	Set on to run the PRESET test within BI/O. If set off, the test is omitted.
11	Set on to suppress all teleprinter messages.
12	Set on to execute another complete diagnostic program cycle.
13	Set on to repeat the routine just ended rather than advance to the next routine.
14	Set on to suppress error halts.
15	Set on to halt at the end of each routine (with the appropriate messages on the teleprinter, to allow a decision to repeat the routine. (See bit 13 to repeat the last test.)

Table 2. Diagnostic Messages

MEMORY DATA	Routine	Message	Comments
102001	BI/O	E1. CLF DID NOT CLEAR FLAG OR SFS CAUSED SKIP WITH FLAG CLEAR	Test the ability to clear the interface flag and test the SFS instruction.
102002	BI/O	E2. SFC DID NOT SKIP WITH FLAG CLEAR	Test the ability of the SFC instruction.
102003	BI/O	E3. STF DID NOT SET FLAG, OR SFC CAUSED SKIP WITH FLAG SET	Test the ability to set interface flag and test the SFC instruction.
102004	BI/O	E4. SFS DID NOT SKIP WITH FLAG SET	Test the SFS instruction
102005	BI/O	E5. DID NOT INTERRUPT	Test the interface interrupt capability.
102006	BI/O	E6. THE RETURN ADDRESS IS NOT CORRECT	The return address that resulted from the interrupt is incorrect.
102007	BI/O	H7. PRESS INTERNAL AND EXTERNAL PRESET, THEN PRESS RUN	Test the PRESET switch(es).
(no halt)	INIT	H8. START RECEIVE(ONLY) INTERFACE DIAGNOSTIC	Message omitted if program option bit 9 set.
102010	BI/O	E1Ø. EXTERNAL PRESET DID NOT SET THE FLAG	PRESET switch(es) failed.
102011	BI/O	H11. END BI-O	Select program options and press RUN.
102012	BI/O	E12. INTERNAL PRESET DID NOT DISABLE INTERRUPTS	PRESET switch(es) failed.
102013	BI/O	E13. EXTERNAL PRESET DID NOT SET FLAG AND INTERNAL PRESET DID NOT DISABLE INTERRUPTS	PRESET switch(es) failed.
102014	BI/O	E14. INTERRUPT ACKNOWLEDGE DID NOT WORK. TEST ABORTED	Remaining tests of BI/O are skipped.
102015	BI/O	E15. CLC Ø DID NOT CLEAR CONTROL FLIP-FLOP	Control bit did not reset with CLC Ø instruction.

Table 2. Diagnostic Messages (cont.)

MEMORY DATA	Routine	Message	Comments
102016	BI/O	E16. PRESET DID NOT CLEAR CONTROL	PRESET switch(es) failed.
102017	BI/O	(none)	CLF Ø did not disable interrupts or SFS Ø caused a bad skip.
102020	BI/O	(none)	CLF Ø did not disable interrupts or SFC Ø did not skip.
102021	BI/O	E21. STF Ø OR SFC Ø DID NOT WORK	STF Ø did not enable interrupts or SFC Ø caused a bad skip.
102022	BI/O	E22. STF Ø OR SFS Ø DID NOT WORK	STF Ø did not enable interrupts or SFS Ø did not skip.
102023	BI/O	E23. CLC ON CHANNEL DID NOT CLEAR CONTROL	Control bit did not reset with CLC CH instruction (CH = interface select code.)
102024	BI/O	E24. CLC CH,C DID NOT CLEAR FLAG OR SFC DID NOT SKIP WITH FLAG CLEAR	This tests the ,C part of the instruction to clear flag.
102025	BI/O	E25. STATUS BITS ARE *xxxxxx* AND SHOULD BE ØØØØØØ	Bits 8 through 15 should be clear. No other bits considered.
102026	BI/O	(none)	First non-TTY display of E25. A- (or switch) Register contains the incorrect status bits.
102027	BI/O	(none)	Second non-TTY display of E25. A- (or switch) Register contains the correct status bits (000000). Press RUN to proceed.
102030	BI/O	(none)	A- (or switch) Register shows current program options. Confirm or change (see Table 1 and press RUN.

Table 2. Diagnostic Messages (cont.)

MEMORY DATA	Routine	Message	Comments
102031	FCTST	E31. INCORRECT STATUS BIT 11 NOT SET	Bit 11 should be set.
102032	FCTST	E32. FLAG NOT SET	Follows test E31.
102033	FCTST	E33. INCORRECT STATUS BIT 11 SET	Bit 11 should be clear.
102034	FCTST	E34. FLAG SET AND SHOULD BE CLEAR	Follows test E33.
102035	FCTST	E35. STATUS BITS ARE *xxxxxx* AND SHOULD BE Ø12ØØØ	Status error.
102036	FCTST	(none)	First non-TTY display of E35. A- (or switch) Register contains the incorrect status bits.
102037	FCTST	(none)	Second non-TTY display of E35. A- (or switch) Register contains the correct status bits (012000).
102040	FCTST	(none)	A- (or switch) Register shows current program options. Confirm or change (see Table 1) and press RUN.
102041	FCTST	E41. FLAG NOT SET	Follows test E35.
102042	FCTST	E42. INCORRECT STATUS. BIT 13 NOT SET	Bit 13 should be set.
102043	FCTST	E43. FLAG SET AND SHOULD BE CLEAR	Follows test E42.
102044	FCTST	E44. STATUS BITS ARE *xxxxxx* AND SHOULD BE Ø2ØØØØ	Status error.
102045	FCTST	(none)	First non-TTY display of E44. A- (or switch) Register contains the incorrect status bits.

Table 2. Diagnostic Messages (cont.)

MEMORY DATA	Routine	Message	Comments
102046	FCTST	(none	Second non-TTY display of E44. A- (or switch) Register contains the correct status bits (020000).
102047	FCTST	(none)	A- (or switch) Register shows current program options. Confirm or change (see Table 1) and press RUN.
102050	FCTST	E5Ø. FLAG NOT SET	Follows test E44.
102051	FCTST	E51. FLAG SET AND SHOULD BE CLEAR	Interface not clearing flag.
102052	FCTST	H52. END FCTST	Select program options and press RUN.
102053	RECVP	E53. ERROR IN RECEIVE PATTERN TEST. *xxxx* PARITY MODE SELECTED, CHARACTER SIZE IS *xx* BITS, WORD RECEIVED WAS *xxxxxx* AND SHOULD BE *xxxxxx*	Interface receive failure. The data received did not compare with the data sent.
102054	RECVP	(none)	First non-TTY display of E53. A- (or switch) Register contains 0 for no-parity mode, 1 for odd-parity mode, or 2 for even-parity mode.
102055	RECVP	(none)	Second non-TTY display of E53. A- (or switch) Register contains the character size in bits.
102056	RECVP	(none)	Third non-TTY display of E53. A- (or switch) Register contains the word sent to the interface.
102057	RECVP	(none)	Fourth non-TTY display of E53. A- (or switch) Register contains the word received.

Table 2. Diagnostic Messages (cont.)

MEMORY DATA	Routine	Message	Comments
102060	RECVP	(none)	A- (or switch) Register shows current program options. Confirm or change (see Table 1) and press RUN.
102061	RECVP	E61. STATUS ERROR IN RECEIVE TEST. STATUS IS *xxxxxx* AND SHOULD BE 1ØØØØØ	Bit 15 should be 1, bit 8 should be 0.
102062	RECVP	(none)	First non-TTY display of E61. A- (or switch) Register contains the incorrect status bits.
102063	RECVP	(none)	Second non-TTY display of E61. A- (or switch) Register contains the correct status bits (100000).
102064	RECVP	(none)	A- (or switch) Register shows current program options. Confirm or change (see Table 1) and press RUN.
102067	RECVP	E67. FLAG NOT SET AFTER RECEIVE CYCLE	Follows tests E53 and E61.
102070	RECVP	H70. END RECVP	Select program options and press RUN.
102073	CFGR	(none)	Confirmation error halt. Enter a valid select code in the switch register then press RUN.
102074	CFGR	(none)	Select internal switch register program options by setting switch register as listed in Table 1 and press RUN.
102077	END	H77. DIAGNOSTIC HAS BEEN COMPLETED	End of test.

Table 2. Diagnostic Messages (cont.)

MEMORY DATA	Routine	Message	Comments
103000	SPCHR	E1ØØ. ERROR IN SPECIAL CHARACTER TEST. *xxxx* PARITY MODE SELECTED, CHARACTER SIZE IS *xx* BITS, DATA WORD IS *xxxxxx*. STATUS RECEIVED IS *xxxxxx* AND SHOULD BE 1Ø1ØØØ	Interface failure
103001	SPCHR	(none)	First non-TTY display of E1ØØ. A- (or switch) Register contains 0 for no-parity mode, 1 for odd-parity mode, or 2 for even-parity mode.
103002	SPCHR	(none)	Second non-TTY display of E1ØØ. A- (or switch) Register contains the character size in bits.
103003	SPCHR	(none)	Third non-TTY display of E1ØØ. A- (or switch) Register contains the word sent to the interface.
103004	SPCHR	(none)	Fourth non-TTY display of E1ØØ. A- (or switch) Register contains the incorrect status bits. Status word should be 101000.
103005	SPCHR	(none)	A- (or switch Register shows current program options. Confirm or change (see Table 1) and press RUN.
103006	SPCHR	E1Ø6. FLAG NOT SET AFTER SPECIAL CHARACTER TEST	Follows test E1ØØ.
103007	SPCHR	E1Ø7. SPECIAL CHARACTER BIT IS SET	The Special Character bit should be clear.
103010	SPCHR	H11Ø. END SPCHR	Select program options and press RUN.

Table 2. Diagnostic Messages (cont.)

MEMORY DATA	Routine	Message	Comments
103025	SYNCH	E125. ERROR IN SYNC CODE TEST. BIT 15 IS NOT SET. *xxxx* PARITY MODE SELECTED, CHARACTER SIZE IS *xx* BITS, DATA WORD IS *xxxxxx*	Bit 15 should be set.
103026	SYNCH	(none)	First non-TTY display of E125. A- (or switch) Register contains 0 for no-parity mode, 1 for odd-parity mode, or 2 for even-parity mode.
103027	SYNCH	(none)	Second non-TTY display of E125. A- (or switch) Register contains the character size in bits.
103030	SYNCH	(none)	Third non-TTY display of E125. A- (or switch) Register contains the word sent to the interface.
103031	SYNCH	(none)	A- (or switch) Register shows current program options. Confirm or change (see Table 1) and press RUN.
103034	SYNCH	E134. FLAG NOT SET AFTER SYNC CODE TEST	Follows test E125.
103037	SYNCH	E137. ERROR IN SYNC CODE TEST. BIT 15 IS SET. *xxxx* PARITY MODE SELECTED, CHARACTER SIZE IS *xx* BITS, DATA WORD IS *xxxxxx*.	Bit 15 should be clear.
103040	SYNCH	(none)	First non-TTY display of E137. A- (or switch) Register contains 0 for no-parity mode, 1 for odd-parity mode, or 2 for even-parity mode.
103041	SYNCH	(none)	Second non-TTY display of E137. A- (or switch) Register contains the character size in bits.

Table 2. Diagnostic Messages (cont.)

MEMORY DATA	Routine	Message	Comments
103042	SYNCH	(none)	Third non-TTY display of E137. A- (or switch) Register contains the word sent to the interface.
103043	SYNCH	(none)	A- (or switch) Register shows current program options. Confirm or change (see Table 1) and press RUN.
103045	SYNCH	H145. END SYNCH	Select program options and press RUN.
103050	LOCKN	E15Ø. BIT 14 NOT SET	Bit 14 should be set when non-sync pattern have been sent to the interface.
103051	LOCKN	E151. FLAG SET AND SHOULD BE CLEAR	Follows test E15Ø.
103052	LOCKN	E152. BIT 14 SET AND SHOULD BE CLEAR	Bit 14 should be clear when two sync patterns have been sent to the interface.
103053	LOCKN	E153. FLAG SET AND SHOULD BE CLEAR	The interface is designed to set flag when data is transferred, but not when sync is recognized. This test follows test E152.
103054	LOCKN	H154. END LOCKN	Select program options and press RUN.
103060	ERRFF	E16Ø. ERROR BIT 8 NOT SET WITH EVEN PARITY CONTROL WORD AND ODD PARITY DATA	Error status bit failed.
103061	ERRFF	E161. ERROR BIT 8 NOT SET WITH ODD PARITY CONTROL WORD AND EVEN PARITY DATA	Error status bit failed.

Table 2. Diagnostic Messages (cont.)

MEMORY DATA	Routine	Message	Comments
103062	ERRFF	E162. ERROR BIT 8 NOT SET WITH TWO DATA TRANSFERS WITHOUT A CLF ON CHANNEL	A CLF instruction (on device select code should separate data received. With this instruction suppressed, the error bit failed.
103063	ERRFF	H163. END ERRFF	Select program options and press RUN.
1060*xx*	(any)	(none)	Trap cell interrupt. P-register = memory address when interrupted, *xx* = the trap cell location.

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